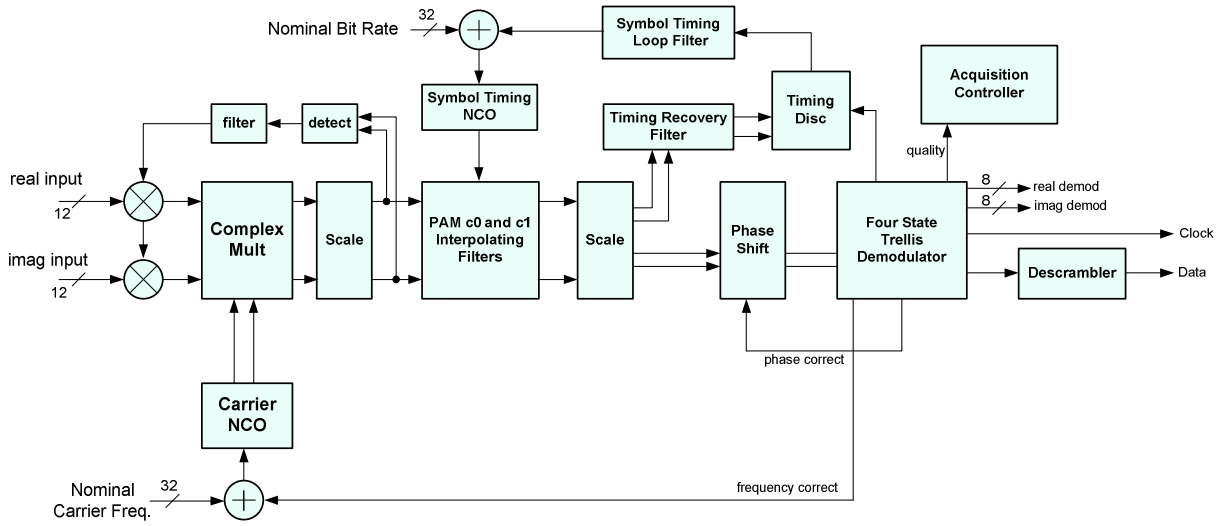
ARTM SOQPSK (Tier 1)
Trellis Demodulator - Verilog Core

Mar 2012



Features

- Compliant with Advanced Range Telemetry (ARTM) tier 1 SOQPSK
- Continuously variable bit rate from less than 50Kbps to 40 Mbps.
- Continuously variable carrier frequency
- Fast acquisition, suitable for telemetry and remote sensing
- SPI interface available
- Non Coherent carrier tracking
- Near-theory demodulation bit error probability to E_b/N_0 below 0dB
- Provides NRZ-L and RNRZ-L outputs..
- Efficient trellis demodulation
- Very simple signal acquisition
- Digital dynamic range of 30-40 dB.
- Carrier frequency acquisition of +/- 12% of bit rate

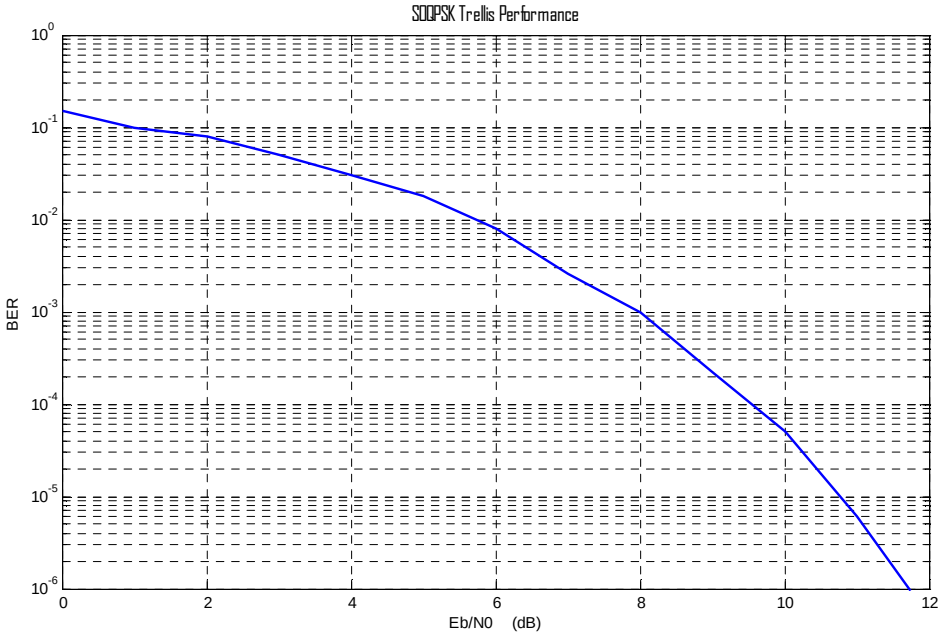
This trellis demodulator IP can be targeted at a low cost FPGA for implementation of a high performance SOQPSK Tier 1 receiver. The efficient Viterbi algorithm is used to provide near theoretical bit-error-probability performance over a wide range of E_b/N_0. The maximum clock rate for Cyclone 4 technology is 125 MHz, with three clock cycles required per bit of information processed. The clock rate can be adjusted for different intermediate frequencies, in direct sampling applications. Baseband inputs are also supported with A/D resolution up to 16 bits.

Custom interfaces (such as I^2C or 3-wire) can be accommodated. Full engineering support provided during product development.

Contact Mike Paff 650 941 2954 (mpaff@paffengineering.com) for more information

FPGA Resource Utilization (Altera Cyclone IV- EP4CE22F17C)

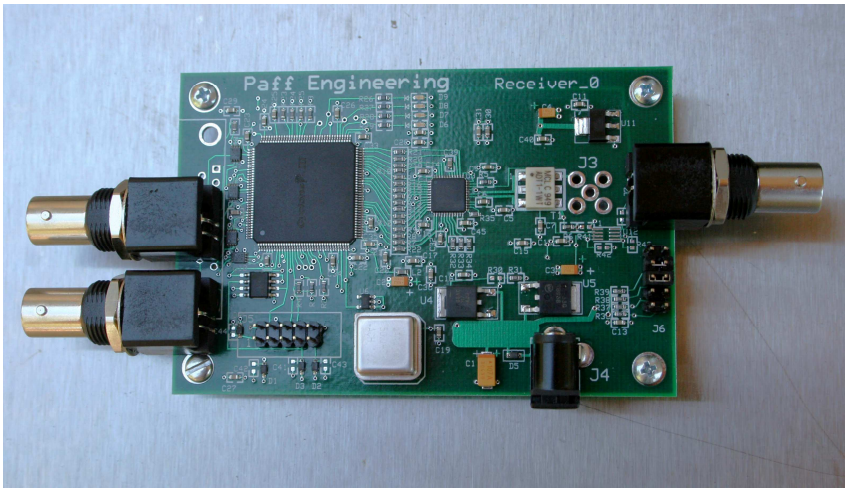
	Logic Cells	ROM (bits)	DSP Elements
Demodulator	11,187	196,608	81



BER Performance

The above performance includes the effects of differential coding and encoding, which is the baseline for the standard. Much published literature does not include this effect.

Evaluation Board



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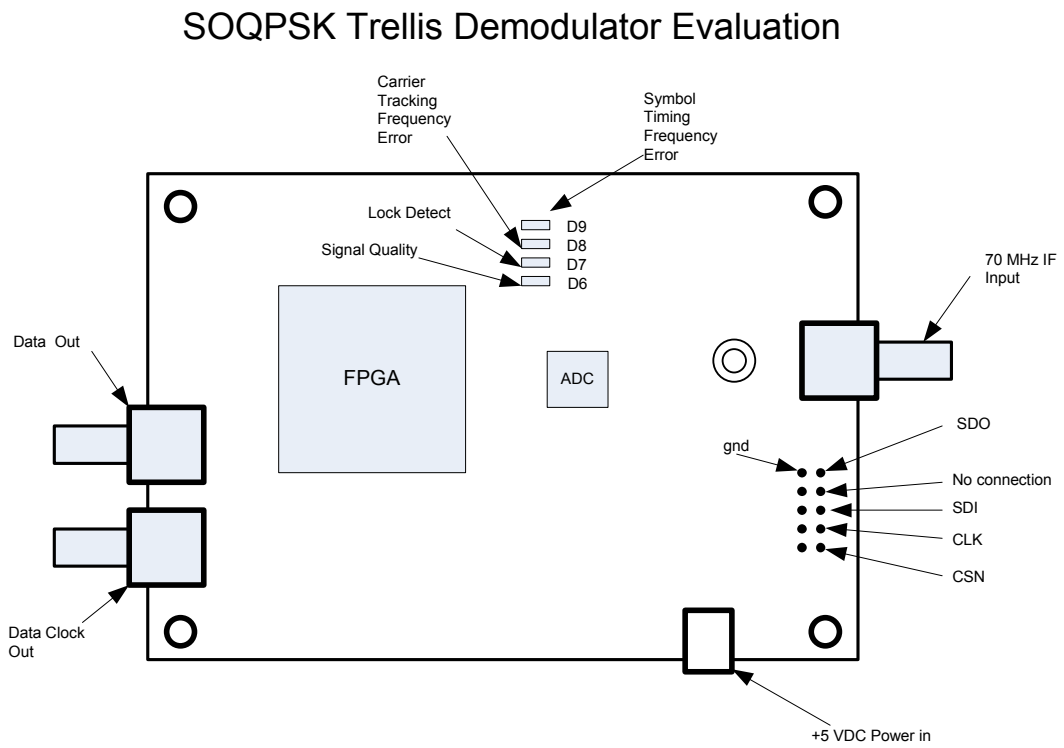
The evaluation board provides a means of testing the existing IP, utilizing an Altera Cyclone 3 FPGA and the Analog Devices AD9233 A/D converter, clocked at 93.3MHz. A bandlimited signal, centered at 70 MHz, is applied to the input port, conforming to the ARTM Tier 1 standard. The board is configurable with an SPI interface. The bit rate range is limited in this single A/D converter implementation to 1/2 the maximum rate of a baseband implementation, which provides digital real and imaginary signals to the demodulator. A practical limit for this configuration is about 15 Mbps.

The signal applied to the evaluation board must be filtered to prevent out-of-band components from being aliased back to the 70 MHz signal passband by the 93.3 MHz clock.



D 6 LED - signal quality indication
D 7 LED - signal quality indication ms bit
D8 LED - flashes at the rate of the carrier frequency error
D9 LED - flashes at the rate of the symbol timing recovery error

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