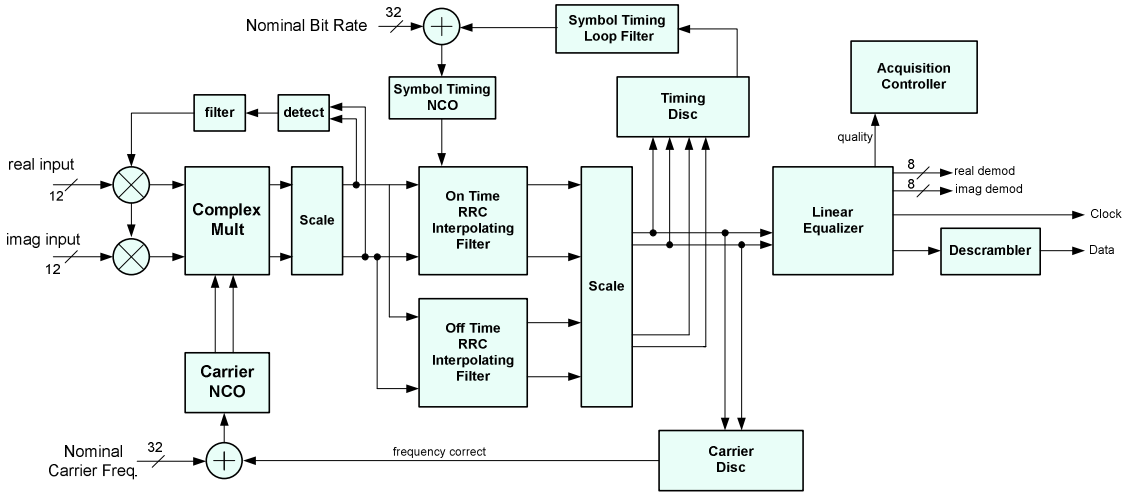
PSK Demodulator - Verilog Core

Aug. 2013



Features

- Processes bandwidth efficient signals which employ RRC filtering.
- Continuously variable bit rate from 10Kbps to 25 Mbps.
- Continuously variable carrier frequency
- Fast acquisition, suitable for telemetry and remote sensing
- Evaluation Board available
- Near-theory demodulation bit error probability to E_b/N_0 below 2dB
- Provides NRZ-L and RNRZ-L outputs..
- Liner Equalizer removes inter-symbol interference – specific performance is a function of bit rate and FPGA size.
- Very simple signal acquisition
- Digital dynamic range of 30-40 dB.
- Carrier frequency acquisition of +/- 20% of bit rate

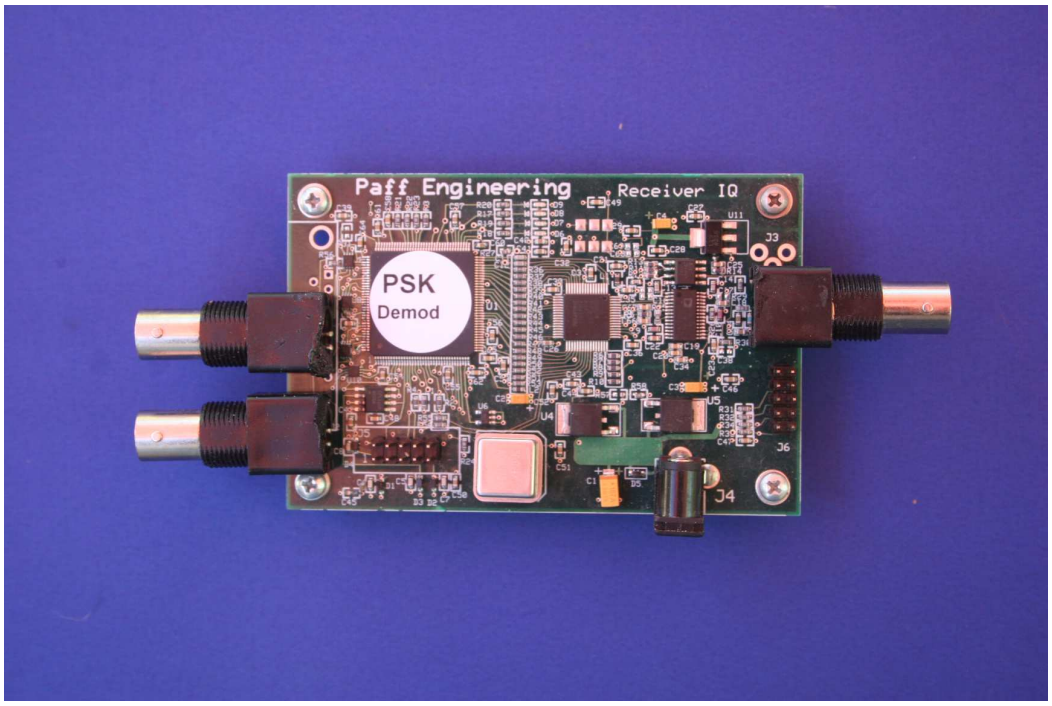
The design is expandable to higher order PSK constellations- up to 256 QAM

FPGA Resource Utilization (Altera Cyclone III - EP3C25E144C)

	Logic Cells	Memory (bits)	DSP Elements
Demodulator	18,429	162,794	154

Contact Mike Paff 650 941 2954 (mpaff@paffengineering.com) for more information

Evaluation Board



The evaluation board provides a means of testing the IP, utilizing an Altera Cyclone 3 FPGA and the Analog Devices AD9233 A/D converter, clocked at 120 MHz. A bandlimited BPSK signal with root raised cosine filtering (25%), centered at 70 MHz, is applied to the input port., A three wire SDI interface allows the user to configure the demodulator bit rate and tracking loop bandwidth for different configurations. The equalizer is set up for a span of 44 symbols (+/- 22) with a maximum bit rate of 10Mbps.

The signal applied to the evaluation board must be filtered to prevent out-of-band components from causing unwanted degradation.

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