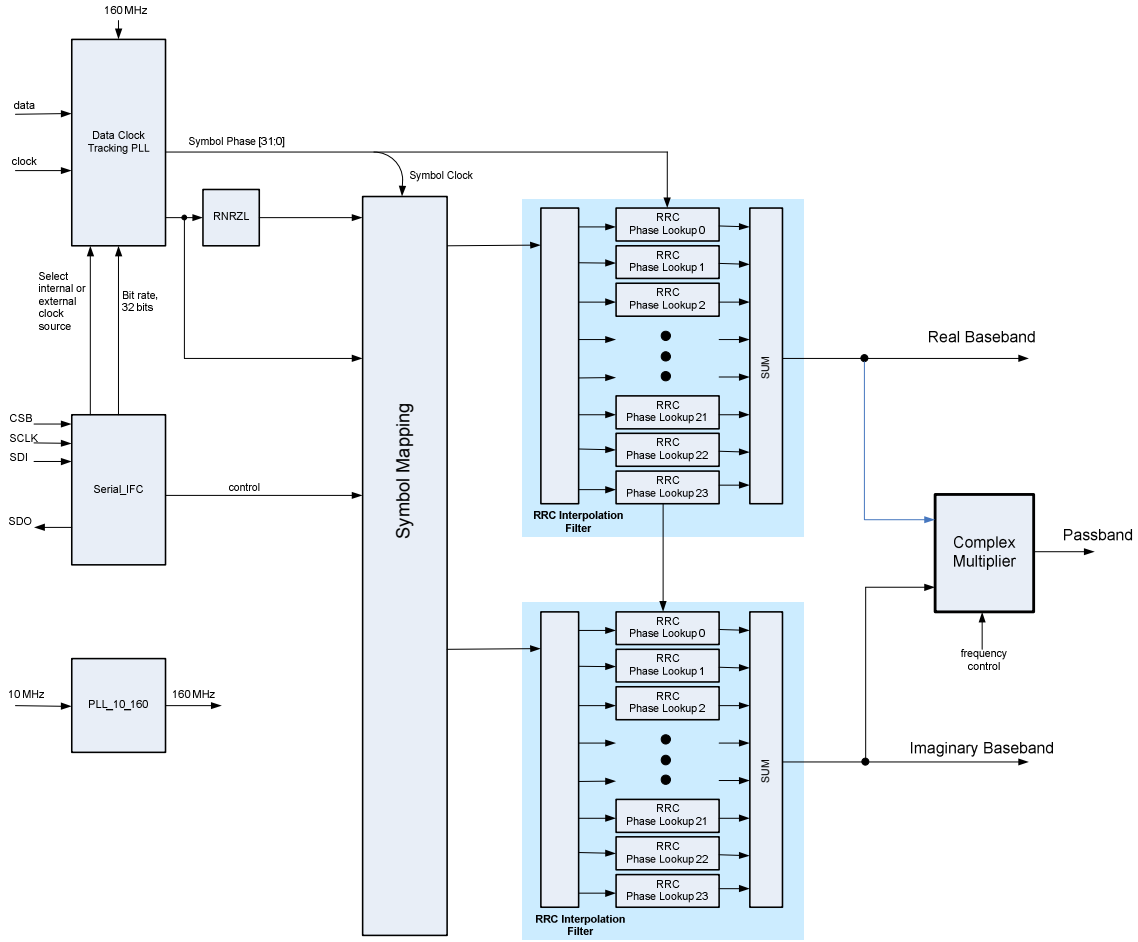
PSK Modulator - Verilog Core

Aug. 2013



Features

- Produces a bandwidth efficient signal employing RRC filtering with length 24T.
- Continuously variable bit rate from 10Kbps to 40 Mbps.
- Continuously variable carrier frequency
- BPSK baseline is expandable to 256 QAM
- Evaluation Board available
- Employs one fixed internal rate clock
- Supports NRZ-L and RNRZ-L outputs.
- FEC options available

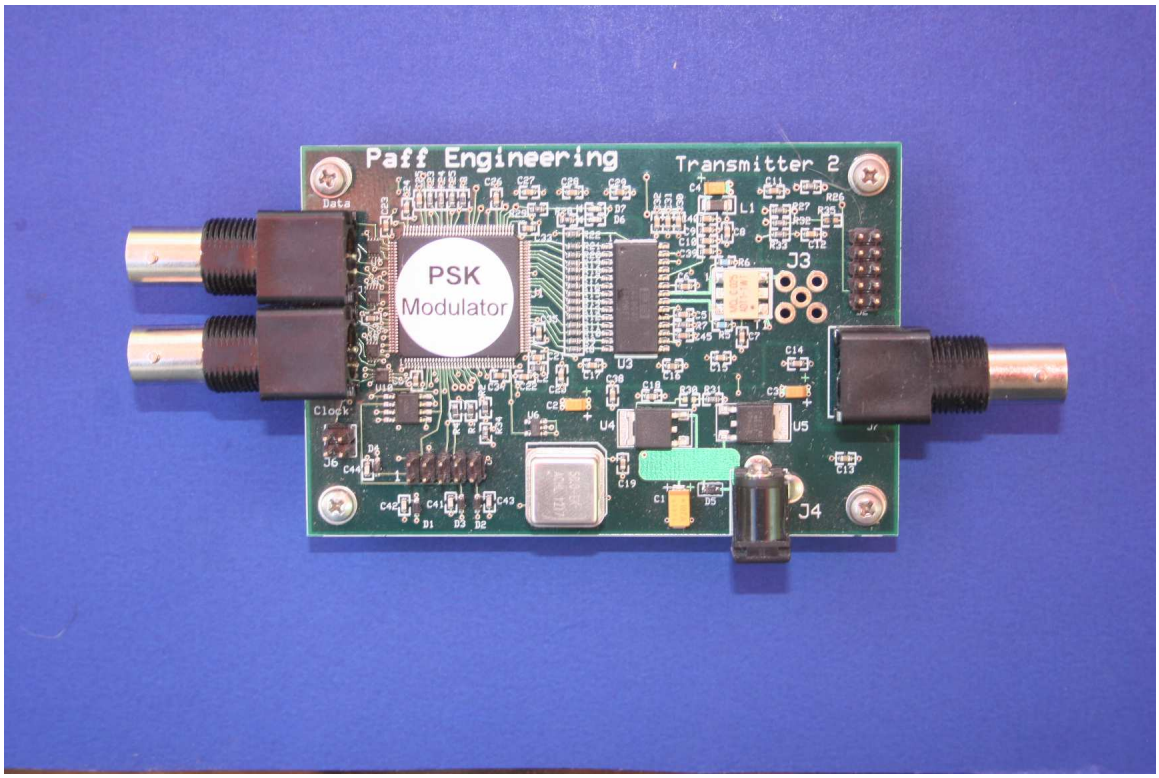
Contact Mike Paff 650 941 2954 (mpaff@paffengineering.com) for more information

Custom interfaces (such as I^2C) can be accommodated. Full engineering support provided during product development.

FPGA Resource Utilization (Altera Cyclone III - EP3C25E144C)

	Logic Cells	Memory (bits)	DSP Elements
BPSK Demodulator	1,730	163,840	8

Evaluation Board

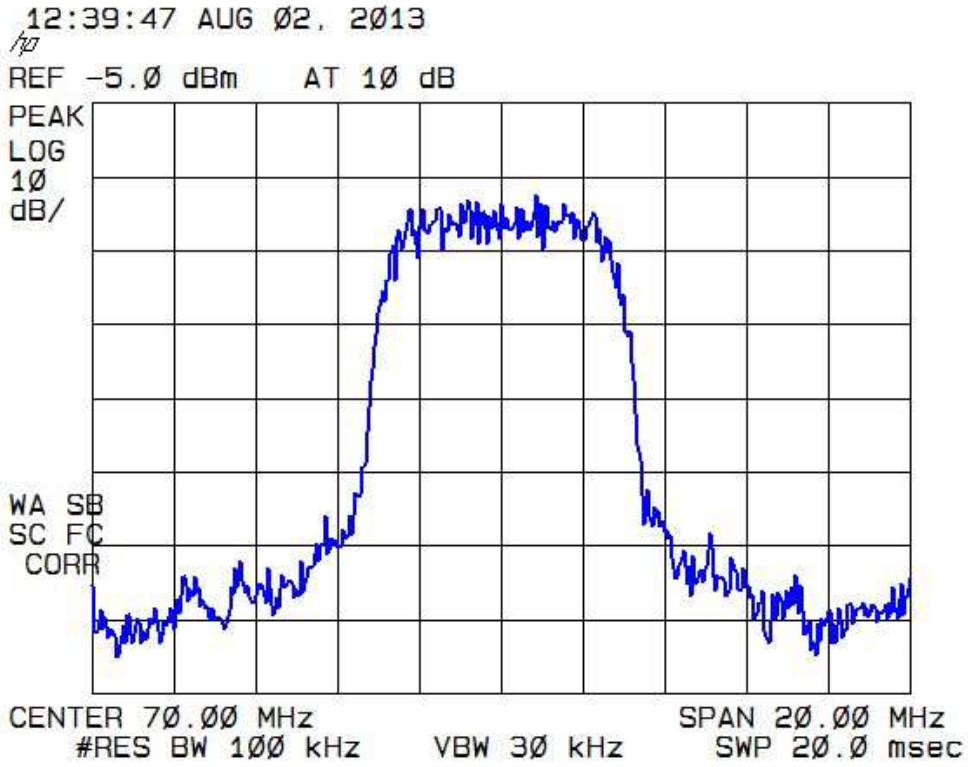


The evaluation board provides a means of testing the IP, utilizing an Altera Cyclone 3 FPGA and Texas Instruments DAC904 converter, clocked at 160 MHz. A bandlimited BPSK signal with root raised cosine filtering (25%), centered at 70 MHz, is provided at the output port., Digital clock and data is applied to the BNC input ports to establish the data rate and the transmit bit pattern.

The signal generated by the evaluation board must be filtered to prevent out-of-band components from causing unwanted degradatio

Contact Mike Paff 650 941 2954 (mpaff@paffengineering.com) for more information

Typical Spectrum Generated by the Evaluation Board (5 MBPS)



Contact Mike Paff 650 941 2954 (mpaff@paffengineering.com) for more information