PCM-FM IQ Demodulator Evaluation Board

Carrier Tracking Frequency Error
(flashes at rate of frequency error)

Symbol Timing Frequency Error
(flashes at rate of frequency error)

Signal Present

Lock Detect

D9
D8
D7
D6

Receiver IQ

IF Input
(70MHz nominal)

Data Out

FPGA

ADC

AD8348

SDO

No connection

SDI

CLK

CSN

gnd

J6

Data Clock
Out

+5 VDC Power in
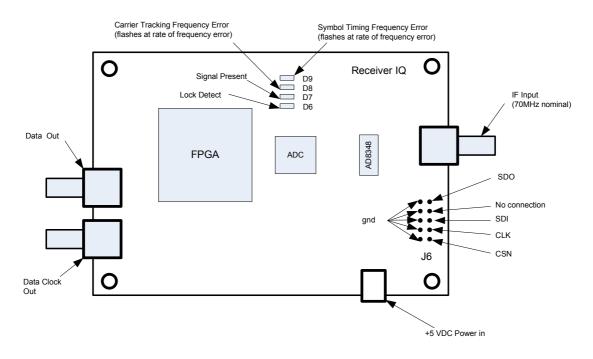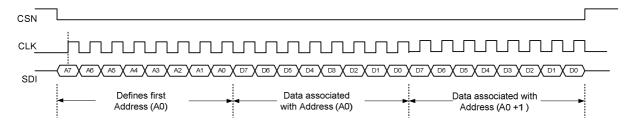
All configuration of the Evaluation Board is done through the SPI interface, which is provided on J6. The nominal IF frequency is 70 MHz, but the board is capable of being configured for any frequency between 50 MHz and 200 MHz.

Three Wire Serial Interface

CSN

CLK

SDI

A7 A6 A5 A4 A3 A2 A1 A0 D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0 D7 D6 D5 D4 D3 D2 D1 D0

Defines first
Address (A0)

Data associated
with Address (A0)

Data associated with
Address (A0 +1)

The format of writing data to the Evaluation board is illustrated above. Data on the SDI line is transferred on the positive transition of CLK when CSN is active low. The CSN line may remain low for transfers of 1 to 8 bytes of data. The most significant bit is sent first in each byte transmission. The address increments by one after each byte is written.

Write Data

address

0	Bit Rate [7:0]
1	Bit Rate [15:8]
2	Bit Rate [23:16]
3	Bit Rate [31:24]
4	Symbol Timing Loop Bandwidth [4:0] , 3 msbs ignored
5	no meaning
6	Bit[0] 1 enables 15 length descrambler
	Bit[1] 1 inverts data out
	Bit[2] 1 inverts data out clock.
	Bit[3] 1 enables internal equalizer
	Bit[4] 1 enables h-tracking function
	Bits [7:5] no meaning
7	Spare

If the target bit rate is BR in units of bits per second, then the parameter Bit Rate is defined as:

$$\text{Bit Rate} = \text{round} ((BR/120*10^6)* 2^{32})$$

For example, assume the target signal has a bit rate of 3.4 M bps. The parameter Bit Rate is 121690740, or 0740DA74 hex. The information provided on the SPI link to configure 3.4 Mbps is

00 74 DA 40 07 hex.

The symbol timing loop bandwidth control is defined as a percentage of the bit rate

control			control	
31	2%		20	0.9%
30	1.9%		19	0.8%
29	1.8%		18	0.7%
28	1.7%		17	0.6%
27	1.6%		16	0.5%
26	1.5%		15	0.4%
25	1.4%		14	0.3%
24	1.3%		13	0.2%
23	1.2%		12	0.1%
22	1.1%		11	0.1%
21	1.0%		10:0	0.1%

Read Data

The format for reading data is the same as writing data with output data provided on the SDO line. The SDI line is only used for sending the start address in the first byte position.

Addresses 64 through 71 are a mirror of date written into addresses 0 through 7.

address

64	programmed Bit Rate [7:0]
65	programmed Bit Rate [15:8]
66	programmed Bit Rate [23:16]
67	programmed Bit Rate [31:24]
68	programmed Symbol Timing Loop Bandwidth
69	zero
70	programmed word 6
71	programmed word 7

72	bit 7	1 = signal present
	bit 6	1 = demodulator lock
	bit 5	1 = Altera PLL locked
	bits 4:0	FPGA version number

73	tracking bit rate [7:0]
74	tracking bit rate [15:8]
75	tracking bit rate [23:16]
76	tracking bit rate [31:24]
77	tracking carrier frequency [7:0]
78	tracking carrier frequency [15:8]
79	tracking carrier frequency [23:16]
80	tracking carrier frequency [31:24]

The four words associated with tracking bit rate must be read together to have meaning. Similarly, the four words associated with tracking carrier frequency must be read together (CSN low for at least five bytes).