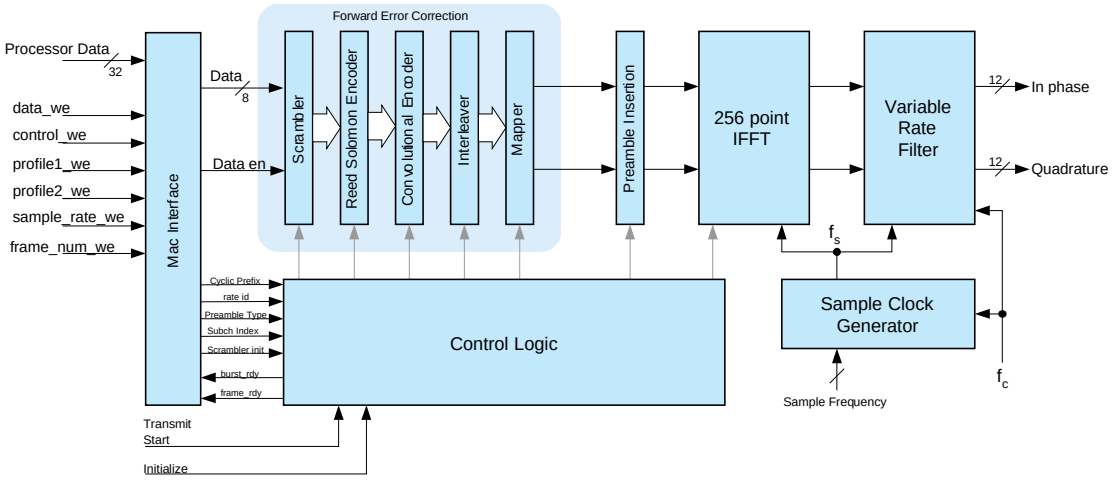
802.16-2004 OFDM Transmitter Baseband PHY

Subscriber Terminal



Features

- Continuously Variable Bandwidth from 1.5 MHz to 28 MHz.
- Subchannelization
- BPSK, QPSK, 16 QAM , 64 QAM
- Seven RS & CC modes
- TDD or FDD
- Bit True Matlab Model available
- 12 bit resolution outputs
- FPGA or ASIC implementation
- Focused Contention Support
- Verilog RTL
- Full or Half Duplex

The transmit logic is designed to clock at a fixed rate of 120 MHz to enable any sample rate from 1.72 MHz (1.5 MHz BW) through 31.92 MHz (28 MHz BW). Power saving can be achieved by lowering the clock frequency, for applications which do not require the highest bandwidth. Bandwidth can be dynamically changed as the transmission frequency is changed from one channel to another.

The 802.16-2004 OFDM standard provides seven different modulation and coding combinations along with the bandwidth flexibility. In addition, the standard supports subchannelization which permits reducing the normal 200 active subcarriers down to any multiple of 12 subcarriers. This flexibility allows the link to provide optimum throughput, depending on the available signal quality at each subscriber.

FPGA Resource Utilization (Altera Stratix II)

	LC Combinationals	RAM & ROM (bits)
Modulator and FEC	3071	47,635
Interpolating Filter	3745	0

Sampling Clock and Spectrum

The transmitter employs an interpolating filter at its output to provide the system designer a great amount of flexibility in selection of the system clock frequency. A fixed frequency system clock can support a wide range of modulation bandwidth conditions. If the symbol period, including cyclic prefix, is T_s, the minimum clock frequency can be expressed:

$$f_{cmin} = 1026/T_s$$

For example, if the cyclic prefix were always ¼, and the bandwidth were 1.5 MHz, the symbol duration would be fixed at 182.046 microseconds resulting in f_{cmin} of 5.636 MHz. If the cyclic prefix could be as short as 1/32, and the bandwidth were 28 MHz, the minimum duration T_s is 8.25 microseconds, resulting in f_{cmin} of 124.12MHz. A Stratix II part will support clock speeds over 150 MHz for this design. By setting the system clock to 125 MHz, any bandwidth between 1.5 MHz and 28 MHz could be supported with any cyclic prefix and any coding rate.

Figure 1 illustrates the interpolators ability to exceed the spectral flatness requirement (+2/-4 dB over the 200 active tones) defined by 802.16-2004. This figure also illustrates the suppression of the first image by 30 dB, which exceeds the ETSI EN 301 021 requirements for system types E, Fand G.

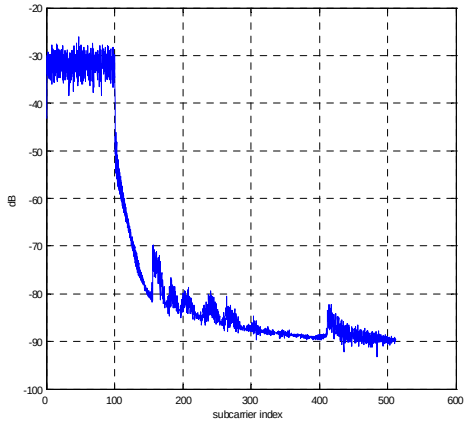


Figure 1 Spectral Flatness and Close-in Spurious

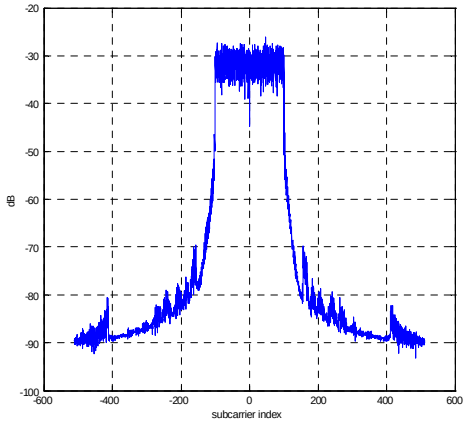


Figure 2 Interpolation Ratio of 4

Figure 2 illustrates the entire spectrum for the case where the clock frequency is four times the sample frequency. The sample frequency for this modulation can be defined as 256 times the subcarrier spacing.

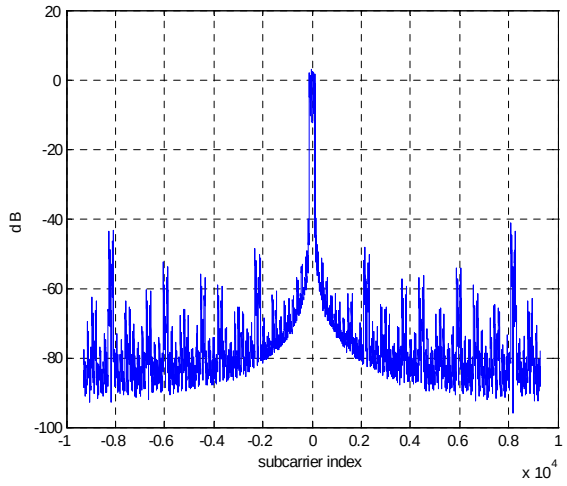


Figure 3 Interpolation Ratio of 72.67

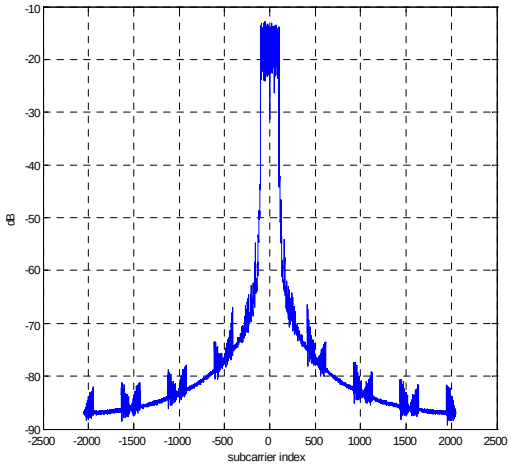


Figure 4 Interpolation Ratio of 16

Figure 3 illustrates the spectrum which would result if the clock frequency were 125 MHz and the sample frequency were 1.72MHz required for a bandwidth of 1.5 MHz. The very high, irrational interpolation ratio results in out of band spurious components which must be removed by external analog filtering.

If possible, the clock should be selected to be close to a binary multiple of the sampling frequency. Figure 4 illustrates the case where this ratio is 16, and the resultant spectrum requires very little analog, post converter filtering.

Relative Constellation Error

The constellation error in 64 QAM mode is -36 dB, as determined by analyzing the bit true baseband signal produced by transmitter. The channel estimation symbol (the second of the two symbol long preamble) was evaluated and interpolated to produce the 192 complex channel estimation values required for data demodulation. The power and variance of each subcarrier of each symbol is computed per equation 97 of IEEE 802.16-2004, following equalization using the interpolated channel estimation values.

The in-band ripple of the transmit filter has a strong influence on the achievable constellation error. If the ripple were as relaxed as the +/- 2dB allowed by the standard, the equalizer performance may be degraded , causing the constellation error to exceed -32dB. The passband ripple for this design is within a 0.5 dB range to allow the equalizer to perform near the theoretical limit.

Interface Signals

The top level timing relationships are illustrated in Figure 5. Each subscriber transmit burst is initiated by *initialize_burst* going true for one clock cycle. At that time, there are 12 set-up parameters which are valid and stored in the transmitter to define all the characteristics of the burst.

At a minimum of 1320 clock cycles following *initialize_burst* going true, the signal *start_transmit* is set to one for one clock cycle. This causes the *transmit_valid* to go true while the *real_out* and *imag_out* outputs are valid. The *transmit_valid* signal should be used to enable an external HPA. The precise time at which the transmission is initiated is controlled by the MAC and MAC interface after interaction with the base station.

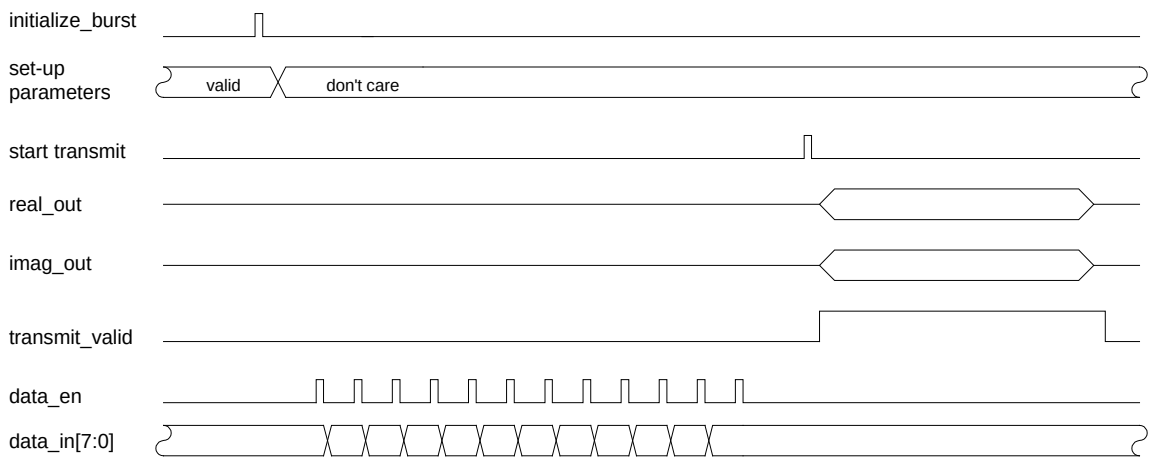


Figure 5 Top Level Timing Interfaces

At any time after *initialize_burst* goes true, the information bytes to be transmitted can be applied to the transmitter. At various places within the transmitter, there are buffer memories capable of storing unprocessed or processed information, These memories are in the Reed Solomon encoder, the interleaver, the IFFT input buffer, the IFFT working buffers and the IFFT output buffer. The transmitter is designed to allow these memories to be filled in an elastic manner, much like a FIFO.

OFDM transmissions are organized into groups of symbols, which are called bursts. All of the symbols associated with one burst have the same modulation and coding characteristics. There are seven possible modulation/coding schemes as defined in table 1.

rate_id	Bytes per Symbol	Modulation	RS Code	CC code
0	11	BPSK	(12,12,0)	1/2
1	23	QPSK	(32,24,0)	2/3
2	35	QPSK	(40,36,2)	5/6
3	47	16 QAM	(64,48,8)	2/3
4	71	16 QAM	(80,72,4)	5/6
5	95	64 QAM	(108,96,6)	3/4
6	107	64 QAM	(120,108,6)	5/6

Table 1 Rate ID Definition

For each burst, the total number of bytes associated with that burst is equal to the number of symbols in the burst, times the associated Bytes per Symbol, as defined in table 1. The host processor will write that number of bytes to the transmitter as an integer number of 32 bit words.

If the number of bytes in a burst is not evenly divisible by four, the last 32 bit word is padded with don't care bits. The 8 most significant bits (31:24) of the first data written to the buffer represent the first byte of the transmission.

Once the data associated with a burst has been written to the data buffer memory, a control word is written to the control buffer which describes the burst. This control word defines the rate_id associated with the burst, the number of symbols in the burst and one bit which defines whether or not a preamble is associated with that burst.

If the terminal is a subscriber terminal, there can only be one burst per frame. In this case, the burst must have a one symbol preamble. A basestation transmission must begin with a two symbol preamble, and each subsequent burst of that frame may or may not begin with a one symbol preamble. The basestation may transmit many bursts in one frame. The first burst transmitted by the base station is always the FCH, which is one symbol in duration and is always coded with rate_id =0. The FCH contains data (Figure 6) which defines the rate_id and the length (in bytes) of the first four bursts which follow the FCH. The lower MAC hardware in the subscriber receiver processes the FCH and uses this information to demodulate the first four bursts following the FCH.

The first burst which follows the FCH in a basestation transmission is a MAP message which describes the characteristics of the fifth burst and all subsequent bursts of that frame.

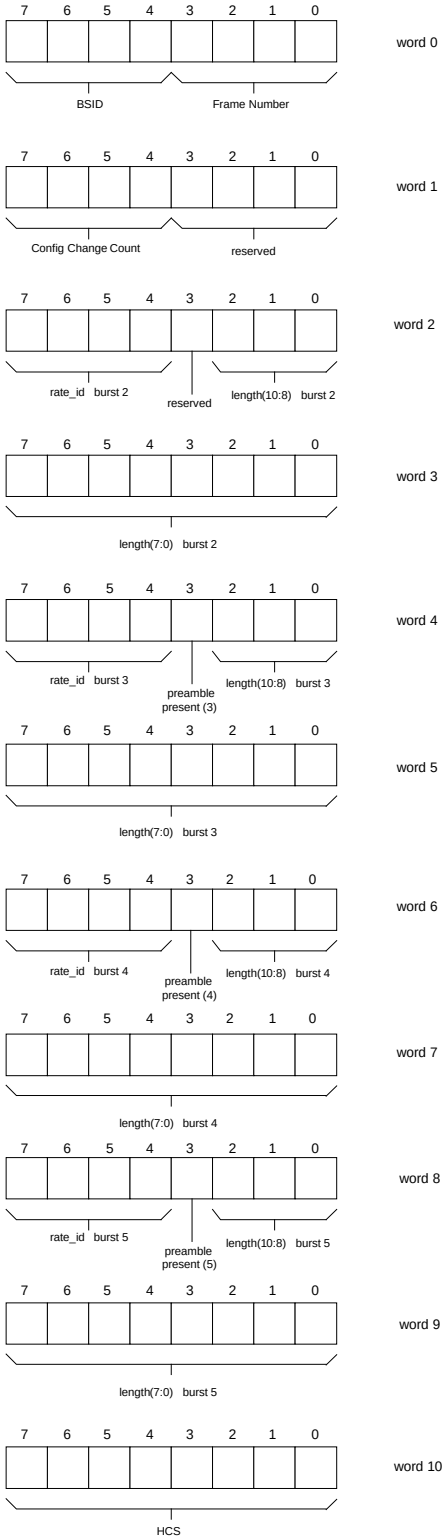


Figure 6 FCH Format

The format of the control word associated with each burst is provided as Figure 7.

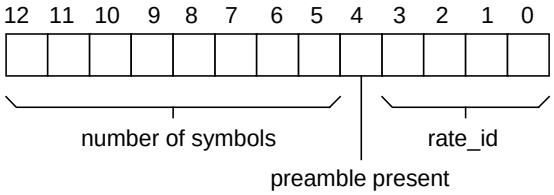


Figure 7 Control Word Format

Each burst transmitted in one frame must be associated with one control word. The FCH control word will always have rate_id =0, preamble present =(don't care), and number of symbols=1. The maximum number of bursts permitted in one frame is TBD.

In addition to the control words, which must be updated each frame, there are three configuration words which must be initialized, but do not change during normal operation. Figure 8 describes the control parameters associated with profile 1.

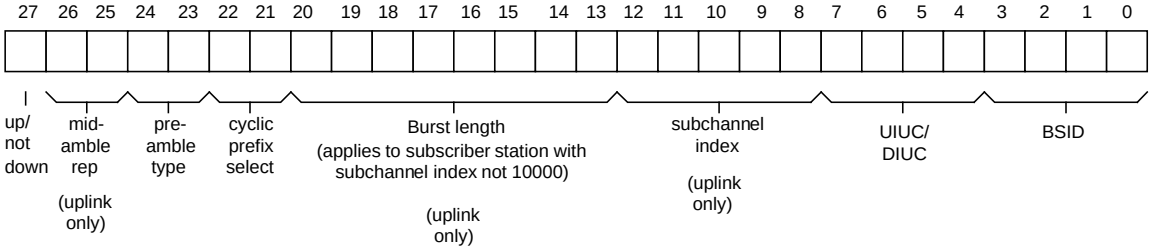


Figure 8 Profile 1 parameters

The parameters associated with profile 2 are illustrated in Figure 9. These parameters pertain to the focused contention mode, which is not implemented in the basestation.

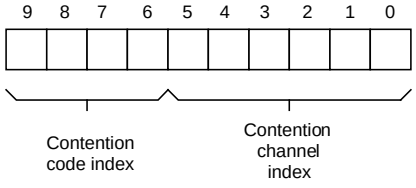


Figure 9 Profile 2 parameters.

The final set-up parameter is the 32 bit sample rate, which must be configured identically in the subscriber and the basestation. This parameter establishes the bandwidth of the signal.

$$\text{ifft sample rate} = f_c \times \text{sample\_rate}/2^{32}$$

where f_c is the clock rate used by the modem logic and sample_rate is the 32 word programmed by the host processor. The ifft_sample_rate cannot be greater than ¼ of the clock rate.

The final parameter to be programmed for each frame is the 4 bit frame number. When this number is programmed into the transmit logic, it is a signal to the transmit logic which initiates the hardware processing associated with that frame.

Figure 10 illustrates the timing of the transmit interface signals to the host processor.

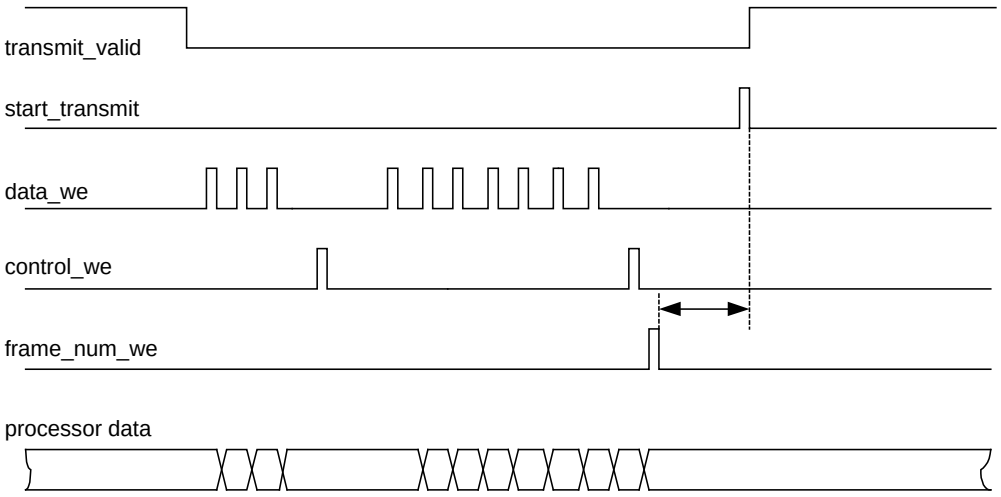


Figure 10 Host Processor Interface to Transmitter Timing

The start_transmit signal which is generated in the timing logic initiates the transmitter logic. When the transmit logic is actively producing a valid output, the transmit_valid signal goes high. The data for the next burst can be entered any time after the transmit_valid associated with the previous burst goes low. This figure illustrates the basestation transmitting two bursts, with the first burst being an FCH consisting of 11 bytes, requiring 3 32 bit data transfers. The second burst is shown with seven data transfers. The transmitter processes the MAC data when frame_num_we goes true. This must go true a minimum of 1320 clock periods before start_transmit goes true. It is possible for the host processor to continue sending data to the transmitter after the transmission has started as long as the transmitter chain is kept full. The transmission will stop when there is no new data available at the ifft output.

Table 2 describes the interface signals to the host processor., and Table 3 describes the primary outputs and Table 4 describes test outputs which can be used for

Signal Name	I/O	width	Description
processor_data	I	32	Processor bus used for writing configuration data to the transmitter and for writing information data for transmission.
data_we	I	1	Goes true for one clock cycle when processor_data is to be written to the input data fifo.
control_we	I	1	Goes true for one clock cycle when processor_data is to be written to the control fifo.

profile_1_we	I	1	Goes true for one clock cycle when the processor data contains the profile 1 information.
profile_2_we	I	1	Goes true for one clock cycle when the processor data contains the profile 2 information.
sample_rate_we	1	1	Goes true for one clock cycle when the processor_data contains the 32 bit sample rate information.
frame_num_we	I	1	Goes true for one clock cycle when the processor_data contains the four bit frame number information
transmit_valid	O	1	Goes true when the transmit output signal is valid. Data associated with the following frame cannot be entered until the current transission has ended.
Start_transmit	I	1	Real time signal which initiates the transmission.
Buff_full	O	1	Goes true when the input fifo is full. The host processor may enter new data (data_en active) when this signal is low.

Table 2 Host Processor Interfaces

Signal name	# of bits	Description
real_out	12	Real baseband output in 2's complement format
imag_out	12	Imaginary baseband output in 2's complement format
transmit_valid	1	Goes to a logic one during the time the baseband output is nonzero, following the *start_transmit* command.
Input_hold	1	When this signal goes true, the transmitter input buffer is full and cannot accept additional input. Once the transmission begins, and the input buffer is emptied, this signal will go low to allow more data to be applied to the transmitter.
transmit_ready	1	This signal goes true approximately 1300 clock cycles following the *initialize_burst* command. The *start_transmit* command cannot be issued until this signal is high.

Table 3 Primary Outputs

Signal name	# of bits	Description
ifft_real_in_d	12	Real baseband input to the ifft in 2's complement format
ifft_imag_in_d	12	Imaginary baseband input to the ifft in 2's complement format
ifft_wr_address_d	8	IFFT write address address 0 corresponds to 0 frequency address 1 corresponds to + delta f address 127 corresponds to +127*delta f address 128 corresponds to -128*delta f address 255 corresponds to -1* delta f
data_in_valid_d	1	IFFT write enable signal
filt_real_in	12	Real input to the interpolating filter. This is the IFFT output with the cyclic prefix added.
filt_imag_in	12	Imaginary input to the interpolating filter. This is the IFFT output with the cyclic prefix added.
filt_in_qual	1	This signal is one with the filter inputs are non-zero

Table 4 Test Signal Outputs

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