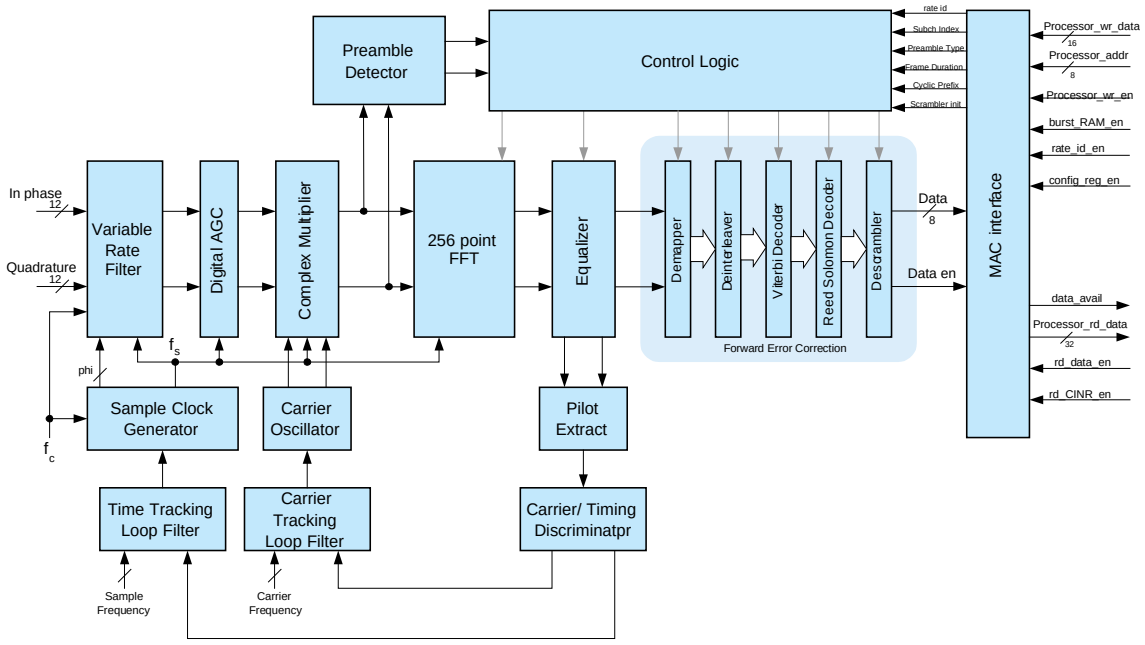
802.16-2004 OFDM Receiver Baseband PHY

Subscriber Terminal



Features

- Continuously Variable Bandwidth from 1.5 MHz to 28 MHz.
- Subchannelization
- BPSK, QPSK, 16 QAM , 64 QAM
- Seven RS & CC modes
- TDD or FDD
- Fixed Sample Rate Input
- 12 bit resolution inputs
- FPGA or ASIC implementation
- Focused Contention
- Verilog RTL
- Full or Half Duplex

A complete, standard compliant, OFDM baseband receiver is implemented in FPGA technology and is capable of operating at full speed in an FPGA test bench. This design is immediately available to integrate with the media access control (MAC) processor. The design does not utilize FPGA DSP resources and may be readily ported to ASIC technology, once full system integration has completed.

The design is ideally suited to fixed point wireless applications, or may be modified for custom applications requiring orthogonal frequency division multiplexing (OFDM) technology.

The receiver may be programmed to support any bandwidth in the range of 1.5 MHz to 28 MHz, utilizing one fixed rate sample clock. Seven different forward error correction modes utilizing concatenated Reed Solomon/ Viterbi decoding are available for additional flexibility.

FPGA Resource Utilization (Altera Stratix II)

	ALUTs	RAM & ROM (bits)
Receiver Total	22778	183779
MAC hardware	428	47424
IFFT	1561	31744
Matched Filter	4839	2624
Decimator	3939	11264
Equalizer	3399	6656
Frequency Translate	1075	18432
Pilot Processor	957	2432
Slicer	254	0
Reed Solomon	4026	12515
Viterbi	1790	33024
Deinterleaver	345	17152
Depuncture	134	512
Descramble	57	0

Although the Stratix II family from Altera is used as the baseline, the design is implemented in generic Verilog and may be ported to other technologies.

The baseband receiver is flexible and may be readily integrated with different receiver front ends. The receiver requires two 12 bit analog to digital (A/D) converters, which are balanced in gain, have good linearity, and the AGC has properly scaled the signal to minimize nonlinear distortion. Furthermore, the receiver assumes that I/Q crosstalk is minimized and there are no large out-of-band interfering signals visible to the A/D converter.

Primary Signal Inputs

Signal name	# of bits	Description
clk	1	Must be a minimum of 4 times the highest IFFT sample rate. The Stratix II logic family will support a clock rate of 140 MHz for this design (speed grade 3).
rst	1	A one on rst forces the logic to an initial state.
real_in	12	Baseband real signal, must be valid at positive edge of clk.
imag_in	12	Baseband imaginary signal, must be valid at positive edge of clk.

Figure 1 illustrates the capability of the receiver to remove out-of-band interference in the digital domain. Good system performance requires both digital domain and analog domain filtering.

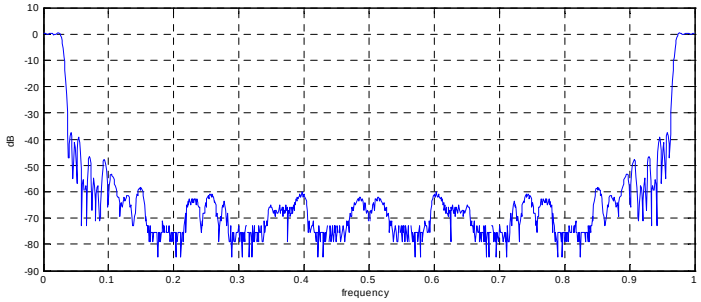


Figure 1a 16:1 Decimation

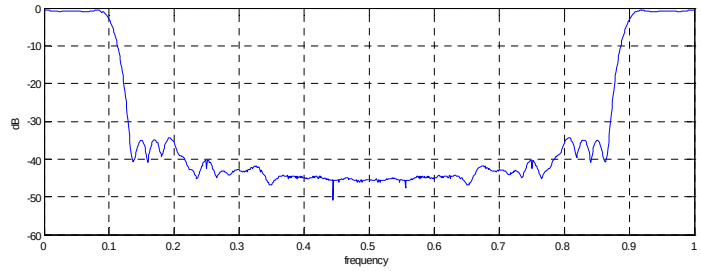


Figure 1b 4.5:1 Decimation

Figure 1 Example Receiver Digital Filtering Characteristics

The baseband receiver is designed to interface directly with a host processor via a 32 bit bus. The host processor must perform initialization of the receiver, implements the MAC layer requirements, and is needed to perform some maintenance functions on a frame-by-frame basis.

Processor Configuration Signal Inputs

Signal name	# of bits	Description
processor_wr_data	32	Processor data bus used for configuring internal registers to the WIMAX receiver.
processor_we	1	This goes to a one for one period of clk, when data is to be written to receiver..
processor_addr	8	Lower bits of processor address bus
Burst_RAM_en	1	When this bit is a one, coincident with processor_we set to one, data is written into the Burst RAM,
rate_id_en	1	When this bit is true, coincident with processor_we set to one, the lookup table which associates DIUC with rate_id is configured.
config_reg_en	1	This signal is set to one when the host processor is writing to the 5 configuration registers (Table 2).

Burst RAM

The Burst RAM is a 16 bit wide, 256 word deep memory which contains the burst profile and length for each burst of the current downlink frame. The first five locations (0 through 4) , contain the description of the first five bursts. The information stored in these locations is written by the MAC hardware and is derived from the received FCH, which is the first burst of the downlink. If there are more than 5 downlink bursts in the frame after the FCH, the description of these bursts is contained in the downlink MAP (DL-map) message, which is the first burst immediately following the FCH. It is the responsibility of the host processor to read the DL-map, and write this information into locations 5 and up. The format of the data to be written to this RAM is described in figure 2.

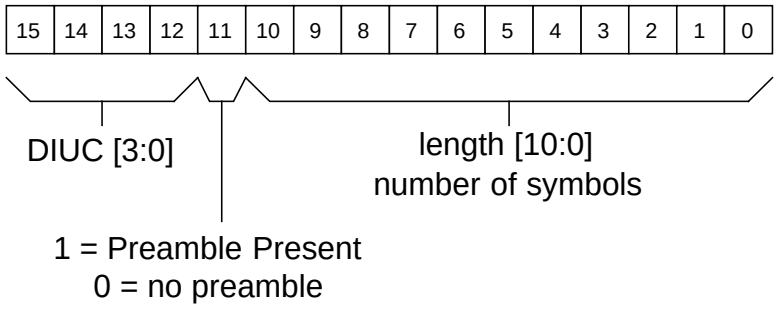


Figure 2 Burst Profile and length

The length term defines the number of symbols in the burst, including the preamble (if present). If no preamble is present, bit 11 is set to zero. The downlink interval usage code (DIUC) which is relevant for the subject burst is defined as the upper 4 bits. Each value of DIUC is associated with one of seven possible rate_id values.

The lookup table which associates DIUC with rate_id is 3 bits wide, by 16 words deep. When, rate_id_en and processor_we are true, the location being written to is defined by the lower four bits of processor_addr. The data written to this memory is the lower three bits of processor_wr_data. This memory must be initialized each time the receiver is powered up, and the information contained in this table is unique to the network. Table 1 defines the meaning of the rate_id term.

rate_id	Bytes per Symbol	Modulation	RS Code	CC code
0	11	BPSK	(12,12,0)	1/2
1	23	QPSK	(32,24,0)	2/3
2	35	QPSK	(40,36,2)	5/6
3	47	16 QAM	(64,48,8)	2/3
4	71	16 QAM	(80,72,4)	5/6
5	95	64 QAM	(108,96,6)	3/4
6	107	64 QAM	(120,108,6)	5/6

Table 1 Rate ID Definition

There are several other parameters which must be initialized before the receiver can begin to process received signals. Most of these parameters are dependent on either the hardware configuration, or the specific network configuration. These parameters are written by the processor during initialization when config_reg_en and processor_we are both active high, in conjunction with the lower bits of processor_addr. Table 2 summarizes these parameters.

Processor addr	bits	Parameter	Parameter Definition
0	32	rate	Defines the IFFT sample rate, which determines the expected bandwidth of the received signal
1	2	cp_sel	Cyclic Prefix Select
2	3	Frame Length	Establishes which of several predefined frame lengths are to be utilized. The received signal must conform to the defined frame length.
3	20	samples_per_20ms	Defines the number of periods of the IFFT sample clock which occur in a period of 20 milliseconds. This parameter is closely tied to the rate parameter.
4	11	Sym_total	Total number of symbols in a downlink frame. For some systems this may be a fixed value, or it may vary from frame to frame. If it does vary, it must be computed by the host processor for each frame.

Table 2 Configuration Parameters

The actual IFFT sample rate (F_s) in the receiver is a function of the 32 bit rate parameter and the frequency of the fixed frequency clk (f_c).

$$F_s = f_c \times rate / 2^{32}$$

In all cases, the lower most bits of the processor_wr_data bus are used to write to the configuration registers.

Table 3 defines the possible frame duration codes.

Code	Frame Duration (ms)	Frames per Second
0	2.5	400
1	4	250
2	5	200
3	8	125
4	10	100
5	12.5	80
6	20	50
7	1	1000

Table 3 Frame Duration Codes

Once the basestation sets the frame duration, it should remain at that value indefinitely. Similarly, the cyclic prefix select (cp_sel), is set when the system is initially installed, and cannot be changed without reconfiguring all the subscriber terminals. Table 4 defines this parameter.

cp_sel	value
0	1/32
1	1/16
2	1/8
3	1/4

Table 4 Cyclic Prefix Values

The cyclic prefix values are defined in terms of the 256 sample, IFFT symbol. When a longer cyclic prefix is selected (such as ¼), the system will exhibit better multipath immunity, at the expense of reduced throughput.

Table 5 describes the host processor interface signals required to read data from the receiver.

Signal name	# of bits	Description
processor_rd_data	32	Data bus driven by the receiver to enable the processor to read data.
data_avail	1	Goes true when the receive FIFO contains received data.
rd_data_en	1	The processor drives this signal to a one for one clock cycle to enable one 32 bit transfer of received data. This signal must be low for a minimum of two clock cycles between the times when it is high. This signal should be driven high only when the data_avail signal is high.
rd_CINR_en	1	The processor drives this signal to a one to read data from a 256 word deep RAM, which contains CINR data from the previous frame. The 8 bit processor_addr defines which of the 256 entries in the RAM is provided on the processor_rd_data bus.
carrier_freq_en	1	The processor drives this signal to a one to read the error in the carrier tracking loop
sym_freq_en	1	The processor drives this signal to a one to read the error in the symbol timing tracking loop

Table 5 Host Processor Interface Signals

Receiver Acquisition

After the receiver has correctly locked to the frame sync, and processed the first 11 byte FCH symbol, the data_available signal is set to one, indicating that receiver data is available to be read from the output FIFO. The 11 bytes are stored in three 32 bit words of the FIFO with the most significant bit of the first word representing the first received bit of the FCH. The last eight bits (bits seven through 0) of the third word have no meaning. The data from each subsequent symbol is always stored in the eight most significant bits of the 32 bit field. If the Reed Solomon coder is employed (rate_id 1 through rate_id 6), the last eight bits of a block of 32 bit words containing data received from one symbol are set to one if the number of errors exceeds the capability of the Reed Solomon decoder, otherwise these 8 bits are set to zero. The data from any symbol always consumes an even number of 32 bit words.

The first burst following the FCH is the DL MAP, which defines the burst profile (DIUC and length in number of symbols) of bursts 6 to the last downlink burst of the frame. The burst profile for bursts one through five is contained in the FCH and processed in hardware. The host processor must read the DL-MAP and load the burst RAM before the fifth burst has finished processing.

The output FIFO is 1024 words deep. The host processor must continually empty the output FIFO as new data is received, without letting the FIFO overflow.

CINR Calculation

The statistics for computing CINR (carrier to interference and noise ratio) are collected for each burst of a subframe and stored in a RAM which is accessible to the host processor. The host processor can read one value, of 19 bit resolution, for each burst of the previous frame, during the time that data is being collected for the current frame. The value read from address 0 corresponds to the CINR measurement of the first burst following the FCH. This capability is

supported for up to 256 bursts in a frame. The following describes how to convert the value read from the RAM (cinr_ram) to CINR in dB:

$$CINR(dB) = 10 \log_{10}(346112/cinr\_ram)$$

Frequency Calibration

The baseband receiver utilizes one fixed frequency clock (clk), and all frequency measurements are based on the frequency of that clock. It is recommended that all oscillators in the RF circuits of the receiver and transmitter be locked to baseband receiver clk. This enables a measurement of the baseband receiver frequency error to be used to compensate for frequency error in the transmitted signal. The uplink signals received by the basestation, from any subscriber, will be locked in frequency to the basestation downlink signal.

When the subscriber receiver is initially turned on, it searches continuously for the first preamble symbol of the frame, which contains 4 repetitions of a time domain waveform of $64/F_s$ in duration (where F_s is the IFFT sampling frequency). After this first preamble symbol is detected, the receiver makes a frequency correction based on the phase angle differences between the 64 sample detections.

Following detection of the first preamble symbol, the receiver detects the second preamble symbol, which consists of 2 repetitions of a time domain waveform of $128/ F_s$ in duration. A fine tuning frequency correction is made, based on the phase angle difference between the two segments of this symbol.

Once the second symbol is detected, the receiver waits for an entire frame to detect the first preamble of the next frame. If this detection happens correctly, then additional frequency corrections are made based on the preamble measurements and lock is declared. Subsequently, the payload is demodulated, and additional carrier frequency corrections are made continuously, based on pilot measurements, as the payload is processed. If the preamble is not detected, the acquisition circuits are reinitialized, the frequency error term is initialized to zero, and the receiver again searches for the downlink preamble.

Once lock is declared, the symbol tracking circuit is enabled, and corrections are made to F_s, based on pilot frequency measurements, once per received symbol. The host processor can read the 32 bit sample clock frequency error (samp_err) by setting sym_freq_en high. The symbol tracking loop error in terms of Hertz is defined as:

$$\Delta F_s = f_c \times (samp\_err)/ 2^{32}$$

where f_c is the system clock frequency.

Similarly, the host processor can read the carrier frequency error (car_err) by setting car_freq_en high. The carrier frequency error in terms of Hertz is:

$$\Delta\omega = F_s \times (car\_err)/ 2^{32}$$

Note that the ability of the receiver to correct carrier frequency error is a function of the IFFT sample frequency. If F_s is the maximum 32 M samples per second (corresponding to 28 MHz bandwidth utilization), the receiver is capable of correcting carrier frequency error up to about 100 KHz. This represents more than 30ppm for a 3 GHz carrier.

If the sample frequency is 1.720 MHz (corresponding to a 1.5 MHz bandwidth utilization), the receiver can only correct for up to about 6 KHz. This is only about 2 ppm for a carrier frequency of 3 GHz. In this case, a very accurate frequency reference is required at the subscriber, or the host processor must implement a frequency search as the first step of acquisition.

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