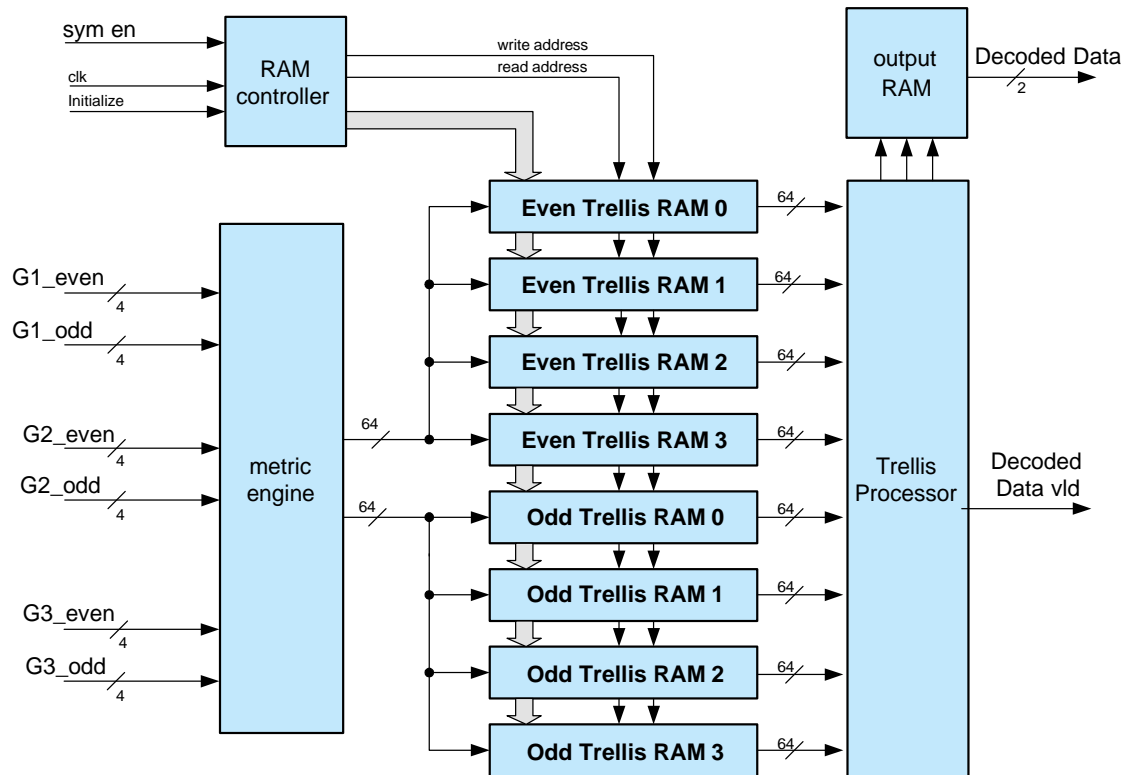


Radix 4 Viterbi Decoder



Features

- Processes two bits per clock period
- 127 bit minimum traceback
- Rate $\frac{1}{2}$ or $\frac{1}{3}$ base code
- 4 bit soft decision
- Matlab Model available
- Greater than 200 M bit per sec
- Most common $K=7$ polynomials
- FPGA or ASIC

This Viterbi decoder is optimized for WIMAX applications, but the polynomials are general enough to support a wide range of different standards (such as DVB). The depuncturing logic and node synchronization logic is standard dependent and must be implemented external to the Viterbi decoder. The minimum traceback length is set to 127 bits, which, along with 4 bit soft decision inputs, provides close to theoretical performance for all conditions, including high puncture rates.

By processing two bits per clock period, the throughput rate is almost doubled compared with a conventional Radix 2 implementation.

FPGA Resource Utilization (Altera Cyclone III)

LC Combinationals

RAM & ROM (bits)

	LC Combinationals	RAM & ROM (bits)
Metric Engine	7656	0
Trellis RAMs	0	32768
Trellis Processor	941	0
Output RAM	0	256

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