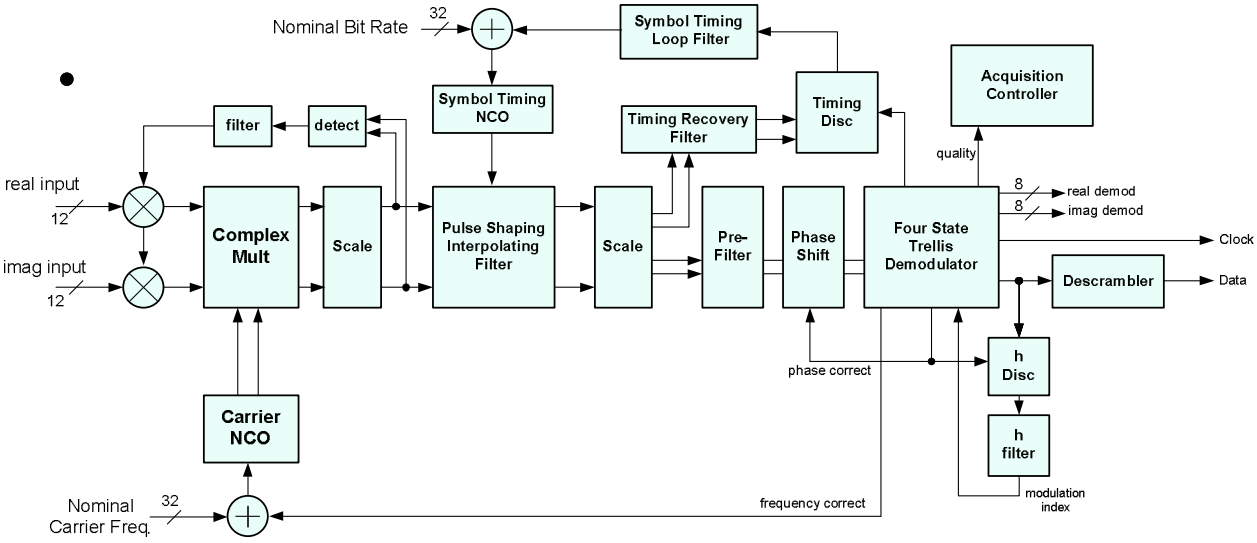
ARTM PSK-FM (Tier 0)
Trellis Demodulator - Verilog Core

Feb 2011



Features

- Compliant with Advanced Range Telemetry (ARTM) tier 0 PCM-FM
- Continuously variable bit rate to 25 Mbps.
- Continuously variable carrier frequency
- Fast acquisition, suitable for telemetry and remote sensing
- Adapts to +/- 10% variation in modulation index (h)
- Non Coherent carrier tracking
- Near-theory demodulation bit error probability to E_b/N_0 below 2dB
- Provides NRZ-L and RNRZ-L outputs..
- Efficient trellis demodulation
- Very simple signal acquisition
- Digital dynamic range of 30-40 dB.
- Carrier frequency acquisition of +/- 12% of bit rate

This trellis demodulator IP can be targeted at a low cost FPGA for implementation of a high performance PCM-FM Tier 0 receiver. The efficient Viterbi algorithm is used to provide near theoretical bit-error-probability performance over a wide range of E_b/N_0. The maximum clock rate for Cyclone 3 technology is 120 MHz, with four clock cycles required per bit of information processed. The clock rate can be adjusted for different intermediate frequencies, in direct sampling applications. Baseband inputs are also supported with A/D resolution up to 16 bits.

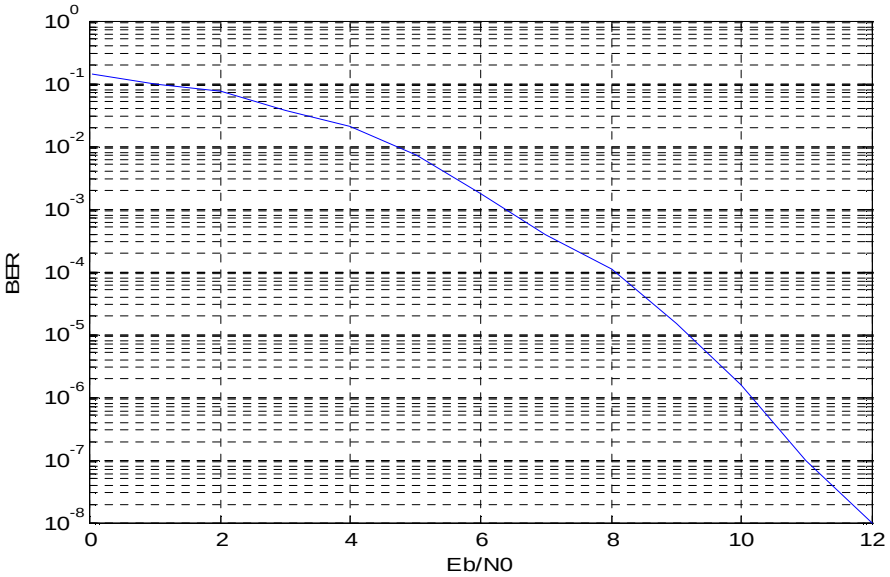
Custom interfaces (such as I^2C or 3-wire) can be accommodated. Full engineering support provided during product development.

Contact Mike Paff 650 941 2954 (mpaff@paffengineering.com) for more information

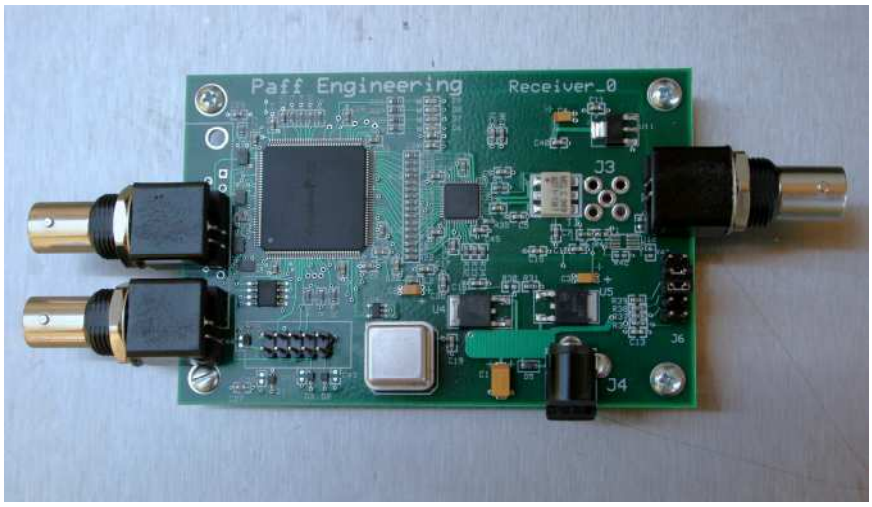
FPGA Resource Utilization (Altera Cyclone III - EP3C25E144C)

	Logic Cells	ROM (bits)	DSP Elements
Demodulator	12849	212992	80

BER Performance



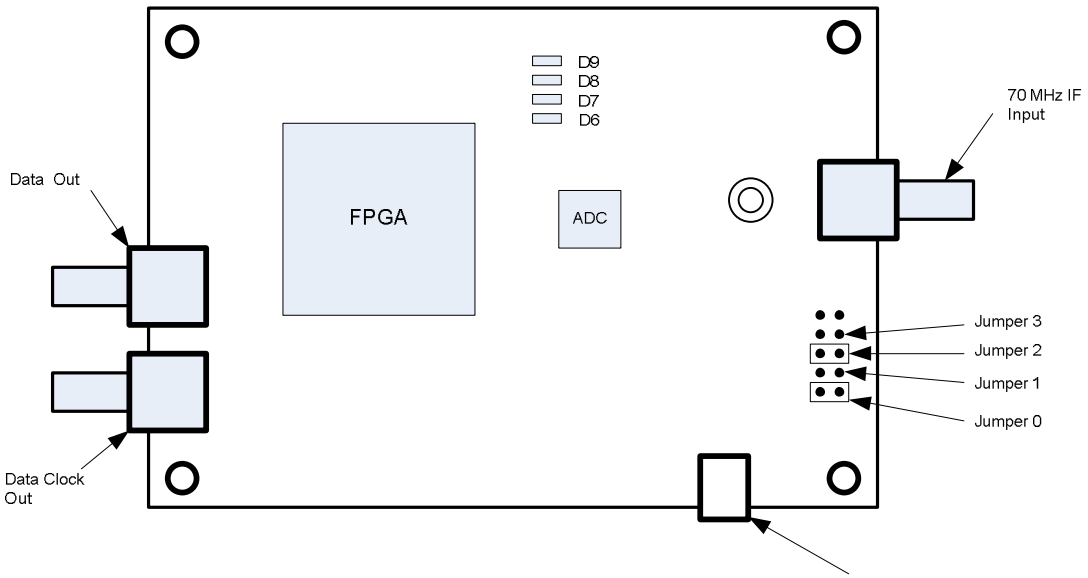
Evaluation Board



Contact Mike Paff 650 941 2954 (mpaff@paffengineering.com) for more information

The evaluation board provides a means of testing the IP, utilizing an Altera Cyclone 3 FPGA and the Analog Devices AD9233 A/D converter, clocked at 93.3MHz. A bandlimited signal, centered at 70 MHz, is applied to the input port, conforming to the ARTM Tier 0 standard, One of 16 possible pre-programmed bit rates is selected by four jumpers on the board. The bit rate range is limited in this single A/D converter implementation to 1/2 the maximum rate of a baseband implementation, which provides digital real and imaginary signals to the demodulator.

The signal applied to the evaluation board must be filtered to prevent out-of-band components from being aliased back to the 70 MHz signal passband by the 93.3 MHz clock.



Jumper 0	Jumper 1	Jumper2	Jumper 3	Bit Rate
in	in	in	in	10 Mbps
out	in	in	in	5 M bps
in	out	in	in	2M bps
out	out	in	in	1 Mbps
in	in	out	in	500 K bps
out	in	out	in	200 K bps
in	out	out	in	100 K bps
out	out	out	in	2.4 Mbps
in	in	in	out	3.42 Mbps
out	in	in	out	3.75 Mbps
in	out	in	out	1.33 Mbps
out	out	in	out	1 Mbps
in	in	out	out	4 Mbps
out	in	out	out	14 Mbps
in	out	out	out	17 Mbps
out	out	out	out	20 Mbps

D 6 LED - signal quality indication
D 7 LED - signal quality indication ms bit
D8 LED - flashes at the rate of the carrier frequency error
D9 LED - flashes at the rate of the symbol timing recovery error

Contact Mike Paff 650 941 2954 (mpaff@paffengineering.com) for more information